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REMARKS

Applicant respectfully requests the Examiner's reconsideration of the present application as amended.

Claims 16, 18, 20-24, 26-27, 33-35, 37-51 are pending in the present application.

Claims 38, and 40-42 are rejected under 35 U.S.C. §102(e) as being unpatentable over U.S. Patent No. 6,907,479 ("Karnstedt").

Claims 16, 18, 20-21, 23-24, 26-27, 33-35, and 37 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,867,727 ("Hattori") in view of U.S. Patent No. 5,557,750 ("Moore") and U.S. Patent No. 6,615,296 ("Daniel").

Claim 22 is rejected under 35 U.S.C. §103(a) as being unpatentable over Hattori in view of Moore and Daniel and Patent Publication 2002/0152263 ("Gordrian").

Claim 39 is rejected under 35 U.S.C. §103(a) as being unpatentable over Karnstedt in view of U.S. Patent No. 6,304,936 ("Sherlock").

Claims 43-46 are rejected under 35 U.S.C. §103(a) as being unpatentable over Karnstedt in view of Gordrian.

Claims 47 and 49-51 are rejected under 35 U.S.C. §103(a) as being unpatentable over Karnstedt in view of U.S. Patent No. 6,891,397 ("Brebner").

Claim 48 is rejected under 35 U.S.C. §103(a) as being unpatentable over Karnstedt in view of Brebner and further in view of Sherlock.

The specification has been amended at page 14 to correct typographical errors.

Support for the amendment to the specification is found on Figures 4 and 5. Applicant submits that no new matter has been added.

Claims 16, 23, 33, 38-39, and 47-48 have been amended.

Support for amended claims 38-39, and 47-48 are found on page 12, lines 9-14 of the specification and in Figure 4 of the drawings. No new matter has been added.

Applicant submits that claims 16, 18, 20-24, 26-27, 33-35, and 37-51 are patentable over Karnstedt, Hattori, Moore, Daniel, Gordrian, Sherlock, and Brebner.

Karnstedt includes a disclosure of integrated circuit FIFO memory devices controlled using a register file, an indexer and a controller. The FIFO memory device includes a FIFO memory that is divisible into up to a predetermined number of independent FIFO queues. The register file includes the predetermined number of words. A respective word is configured to store one or more parameters for a respective one of the FIFO queues. The indexer is configured to index into the register file, to access a respective word that corresponds to a respective FIFO queue that is accessed. The controller is responsive to the respective word that is accessed, and is configured to control access to the respective FIFO queue based upon at least one of the one or more parameters that is stored in the respective word. Thus, as the number of FIFO queues expands, the number of words in the register file may need to expand, but the controller and/or indexer need not change substantially. The register file may include multiple register subfiles, and the controller may include multiple controller subblocks (Karnstedt Abstract).

Hattori includes a disclosure of data transferred via FIFO memories on a word unit basis. The FIFO memory is designated by an upper bit portion of a write address. An ID bit indicating whether a transfer word indicates a command or parameters is allocated to a lower bit portion and is written into the FIFO memory together with inherent word data. Upon reading, a lower bit portion of a read address is compared with the ID bit read out from the FIFO memory. When they don't coincide, the presence of an error is decided. In case of adding redundant bits to the transfer word and judging a loss of word, on the transmission side, transmission side judgment bits having a fixed bit arrangement 01 of two bits are added to each word. Further, with respect to the m-th word, the transmission side judgment bits are shifted by (m-1) bits and a bit arrangement is changed and the resultant data is transmitted. On the reception side, the transmission side judgment bits are reversely shifted to the original positions and three bits in which one bit adjacent to the transmission side judgment bits was added thereto are checked.

When a bit arrangement of the reception side judgment bits corresponding to the transmission side judgment bits coincides with a bit arrangement of the transmission side judgment bits, it is determined that there is no word loss. When they don't coincide, it is decided that there is a word loss (Hattori Abstract).

Moore includes a disclosure of a single chip peripheral bus adapter circuit has a pair of input and output first in, first out (FIFO) buffers, a main buffer, and a pair of supporting registers. The registers increase the performance of the circuit by eliminating or reducing wait states (Moore Abstract).

Daniel includes a disclosure of reducing FIFO access cycles across a system bus in a multi-processor system in which two processors communicate across a system bus through a FIFO, two separate FIFO descriptors are provided. The first descriptor is maintained by the processor located on-board with the FIFO, and the second descriptor is maintained by an off-board processor which communicates with the FIFO across the bus. When one processor performs a FIFO operation, the processor updates the other processor's descriptor via a memory access across the bus. Additionally, one module passes credits to the other to indicate that the latter has permission to perform a plurality of FIFO operations consecutively. In one embodiment a special non-valid data value is used to indicate an empty FIFO position (Daniel Abstract).

Gordrian includes a disclosure of a method and system for switching information packets through a m input, n output device. According to the invention it is proposed to temporarily buffer said packets according to a new, self-explanatory, preferred a linear addressing scheme in which a respective buffer location of consecutive stream packets results from a respective self-explanatory, or linear, respectively, incrementation of a buffer pointer. Preferably, a matrix of FIFO storage elements (10,11,12,13) having an input and an output crossbar can be used for implementing input/output paralleling modes (ILP,OLP) and multiple lanes and achieving address input/output scaling up to a single cycle (Goldrian Abstract).

Sherlock includes a disclosure of a one-to-many bus bridge that includes a system bus interface, a first I/O bus interface, a second I/O bus interface, a multiple logical FIFO system wherein first and second logical FIFOs share a common storage system, and demultiplexer and control circuitry. The demultiplexer and control circuitry are configured so that cycle information destined for the first I/O bus interface is enqueued from the system bus interface into the first logical FIFO and is dequeued from the first logical FIFO into the first I/O bus interface. Cycle information destined for the second I/O bus interface is enqueued from the system bus interface into the second logical FIFO and is dequeued from the second logical FIFO into the second I/O bus interface. A level-of-fullness monitor monitors the common storage system and generates first and second level-of-fullness indications responsive thereto. The system bus interface is operable to declare I/O halt and I/O resume conditions on a system bus responsive to halt and resume commands. The control circuitry issues the halt command when the first level-of-fullness indication is generated, and issues the resume command when the second level-of-fullness indication is generated. The first level-of-fullness indication is generated before the free storage capacity in the common storage system becomes less than a predetermined maximum size of post-halt cycle information. The second level-of-fullness indication is generated after the amount of free storage capacity in the common storage system becomes greater than the predetermined maximum size of the post-halt cycle information (Sherlock Abstract).

Brebner includes a disclosure of an apparatus for a network and a system on a single programmable logic device. The programmable logic includes port modules. The port modules have configurable logic configured to process communications for routing communications. The port modules are configured to the process communications for at least one of a plurality of protocols (Brebner Abstract).

Applicant submits that Karnstedt, Hattori, Moore, Daniel, Gordrain, Sherlock, and Brebner do not teach or suggest <u>a memory read manager to tie assert read enable inputs of the FIFO memories and to select a first FIFO memory to output first data stored in a first storage</u>

element in the first FIFO memory in response to a first read address from a data reading device, wherein the first data was prepared for output prior to a generation of the first read address.

On the contrary, Karnstedt discloses integrated circuit FIFO memory devices having a read enable input, REN (Karnstedt col. 10, lines 32-34, and Figure 2). The read enable, however, is not tie asserted. Instead, the read enable input may be either asserted or deasserted (HIGH or LOW) (Karnstedt col. 10, lines 54-57).

Furthermore, the Office Action mailed 11/15/2006 states that

> In regard to claim 38 Karnstedt teaches:
>
> a memory read manager to select a first FIFO memory to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device (e.g., Read Control Logic 22 and Output MUX 170 in Fig. 2B), wherein the first data was prepared for output prior to a generation of the first read address (e.g., column 10, lines 58-61; column 14, lines 13-19)

(11/15/2006 Office Action, pp. 2-3).

Applicant wishes to point out that column 10, lines 58-61 discloses that when a queue is selected, a next word available in that queue will fall through to output register 264, not a word in a subsequent or other queue. Each queue has a single address (Karnstedt col. 10, lines 24-25). Thus, when a queue is selected with a read address, the "next word" that falls through to the output register is NOT prepared for output prior to a generation of its associated read address, but after generation of its associated read address.

Hattori only discloses a system for judging read out transfer word by comparing flag or transfer word and lower bit portion of destination selection address. Hattori does not teach or suggest a memory read manager to tie assert read enable inputs of the FIFO memories and to select a first FIFO memory to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device, wherein the first data was prepared for output prior to a generation of the first read address.

Moore only discloses a prefetech/prestore mechanism for peripheral controllers with a shared internal bus. Moore does not teach or suggest a memory read manager to tie assert read enable inputs of the FIFO memories and to select a first FIFO memory to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device, wherein the first data was prepared for output prior to a generation of the first read address.

Daniel only discloses an implementation of first-in-first-out memories for mutli-processor systems. Daniel does not teach or suggest a memory read manager to tie assert read enable inputs of the FIFO memories and to select a first FIFO memory to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device, wherein the first data was prepared for output prior to a generation of the first read address.

Goldrain only discloses a control logic implantation for a non-block switch network. Goldrain does not teach or suggest a memory read manager to tie assert read enable inputs of the FIFO memories and to select a first FIFO memory to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device, wherein the first data was prepared for output prior to a generation of the first read address.

Sherlock only discloses a one-to-many bus bridge using independently and simultaneously selectable logical FIFOs. Sherlock does not teach or suggest a memory read manager to tie assert read enable inputs of the FIFO memories and to select a first FIFO memory to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device, wherein the first data was prepared for output prior to a generation of the first read address.

Brebner only discloses a gigabit router on a single programmable logic device. Brebner does not teach or suggest a memory read manager to tie assert read enable inputs of the FIFO memories and to select a first FIFO memory to output first data stored in a first storage element

in the first FIFO memory in response to a first read address from a data reading device, wherein the first data was prepared for output prior to a generation of the first read address.

In contrast, claim 38, as amended, states

> A data buffering unit, comprising:
> a memory that includes a plurality of first-in-first-out (FIFO) memories to store data;
> a memory read manager to tie assert read enable inputs of the FIFO memories and to select a first FIFO memory to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device, wherein the first data was prepared for output prior to a generation of the first read address.

(Claim 38, as amended) (Emphasis added).

Claim 47, as amended, includes similar limitations. Given that claims 39-46, and 48-51 depend from claims 38 and 47, it is likewise submitted that claims 39-46, and 48-51 are also patentable under 35 U.S.C. §102(e) and §103(a) over Karnstedt, Hattori, Moore, Daniel, Goldrain, Daniel, and Brebner.

Applicant further submits that Hattori, Moore, Daniel, Karnstedt, Gordrain, Sherlock, and Brebner do not teach or suggest selecting a first FIFO memory from a plurality of first-in-first-out (FIFO) memories to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device, wherein the first data was prepared for output prior to a generation of the first read address from the data reading device, and preparing next data from a next storage element from the first FIFO memory for output by transmitting a read address of the next storage element to the first FIFO memory prior to a request for the next data from the data reading device.

The Office Action mailed 11/15/2006 states that

> Moore teaches "wherein the first data was prepared for output prior to a generation of the first read address from the data reading device;" (e.g., column 7, lines 66-67 to column 8, lines 1-3; Fig. 2) For preparing the next data for prefetching within a clock cycle.
> Daniel teaches: "preparing next data from a next storage element from the first FIFO memory for output by transmitting a

> read address of the next storage element to the first FIFO memory prior to a request for the next data from the data reading device ..." (e.g., see column 5, lines 63-64) For providing FIFO descriptor including a Read Pointer (RP) (e.g., read address to a FIFO location) pointing to the net location within the FIFO to be read.

(11/15/2006 Office Action, p. 5).

Moore discloses a pre-fetch register 135 which lies between a host and a main FIFO 132. Data in this register 135 is fetched from the main FIFO 132 during available internal data bus cycles. This allows the data to be available when the host requests it. Applicant submits that the pre-fetch register 135 is operable to pre-fetch data from only a single FIFO such as main FIFO 132, not a plurality of FIFO memories as required by the claimed invention (Moore col. 1, line 67 through col. 2, line 7, col. 3, lines 54-62). Moore does not teach or suggest selecting a first FIFO memory from a plurality of FIFO memories to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device, wherein the first data was prepared for output prior to a generation of the first read address from the data reading device.

Daniel discloses providing an RD pointer that points to a next location within a FIFO to be read from. The RD pointer is maintained by an off-board processor which communicates with the FIFO across the bus (Daniel Abstract, col. 4, lines 40-49, and col. 6, lines 34-37). The RD pointer is a request for next data from a data reading device. Thus, Daniel does not disclose preparing next data for output prior to a request for the next data from the data reading device. Furthermore, the techniques described in Daniel are also operable only with a single FIFO, not a plurality of FIFO memories as required by the claimed invention (Daniel Figures 3A-3F and 4A-4F). Daniel also does not teach or suggest selecting a first FIFO memory from a plurality of FIFO memories to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device, wherein the first data was prepared for output prior to a generation of the first read address from the data reading device.

The Office Action mailed 11/15/2006 acknowledges that Hattori does not teach preparing data for output prior to generating a read address from a data reading device, and preparing next data from a next storage element from a FIFO memory for output by transmitting a read address of the next storage element to the FIFO memory prior to a request for the next data from the data reading device (11/15/2006 Office Action, p. 5).

Karnstedt only discloses integrated circuit FIFO memory devices that are divisible into independent FIFO queues, and systems and methods for controlling the same. Karnstedt does not teach or suggest selecting a first FIFO memory from a plurality of FIFO memories to <u>output first data</u> stored in a first storage element in the first FIFO memory <u>in response to a first read address from a data reading device, wherein the first data was prepared for output prior to a generation of the first read address from the data reading device</u>, and <u>preparing next data from a next storage element from the first FIFO memory for output by transmitting a read address of the next storage element to the first FIFO memory prior to a request for the next data from the data reading device</u>.

Goldrain only discloses a control logic implantation for a non-block switch network. Goldrain does not teach or suggest selecting a first FIFO memory from a plurality of FIFO memories to <u>output first data</u> stored in a first storage element in the first FIFO memory <u>in response to a first read address from a data reading device, wherein the first data was prepared for output prior to a generation of the first read address from the data reading device</u>, and <u>preparing next data from a next storage element from the first FIFO memory for output by transmitting a read address of the next storage element to the first FIFO memory prior to a request for the next data from the data reading device</u>.

Sherlock only discloses a one-to-many bus bridge using independently and simultaneously selectable logical FIFOs. Sherlock does not teach or suggest selecting a first FIFO memory from a plurality of FIFO memories to <u>output first data</u> stored in a first storage element in the first FIFO memory <u>in response to a first read address from a data reading device,</u>

wherein the first data was prepared for output prior to a generation of the first read address from the data reading device, and preparing next data from a next storage element from the first FIFO memory for output by transmitting a read address of the next storage element to the first FIFO memory prior to a request for the next data from the data reading device.

Brebner only discloses a gigabit router on a single programmable logic device. Brebner does not teach or suggest selecting a first FIFO memory from a plurality of FIFO memories to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device, wherein the first data was prepared for output prior to a generation of the first read address from the data reading device, and preparing next data from a next storage element from the first FIFO memory for output by transmitting a read address of the next storage element to the first FIFO memory prior to a request for the next data from the data reading device.

In contrast, claim 16 states

> A method for managing data, comprising:
> selecting a first first-in-first-out (FIFO) memory from a plurality of FIFO memories to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device, wherein the first data was prepared for output prior to a generation of the first read address from the data reading device; and
> preparing next data from a next storage element from the first FIFO memory for output by transmitting a read address of the next storage element to the first FIFO memory prior to a request for the next data from the data reading device.

(Claim 16) (Emphasis Added).

Claims 23, 38, and 47 include similar limitations. Claim 33 includes the limitation regarding preparing next data. Given that claims 18, and 20-22 depend from claim 16, claims 24, 26, and 27 depend from claim 23, claims 34-35, and 37 depend from claim 33, and claims 39-46 depend from claim 38, and claims 48-51 depend from claim 47, it is likewise submitted that claims 18, 20-22, 24, 26, 27, 34-35, 37, 39-46, and 48-51 are also patentable under 35 U.S.C. §102(e) and §103(a) over Karnstedt, Hattori, Moore, Daniel, Goldrain, Daniel, and Brebner.

In view of the amendments set forth herein, it is respectfully submitted that the applicable rejections and have been overcome. Accordingly, it is respectfully submitted that claims 16, 18, 20-24, 26-27, 33-35, 37-51 should be found to be in condition for allowance.

If any additional fee is required, please charge Deposit Account No. 50-1624.

Respectfully submitted,

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